23

Feedback extends sequence of random-number generator

by J. T. Harvey
AWA Research Laboratory, New South Wales, Australia

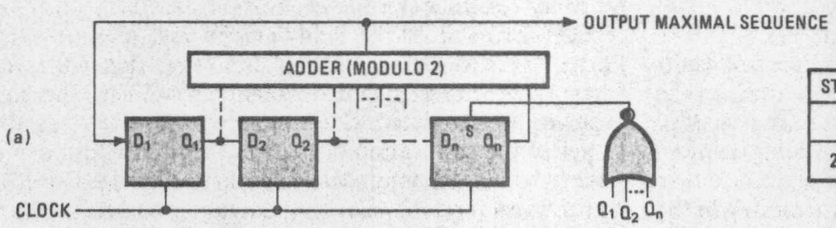
Altering the periodicity of its sequence from 2^{n-1} to 2^n makes a pseudorandom number generator more useful in such applications as frame synchronization, numbering, or identification in a digital communications system. The modification has little effect on the pseudorandomness of the number sequence, and it can be implemented with just a simple shift register and a slightly changed feedback loop.

The usual pseudorandom, or maximal-sequence, generator is shown in (a). It combines a simple feedback circuit with a shift register having a serial output that (in the binary case) is a modulo 2 sum of the nth stage output and one or more of the previous stage outputs. No matter what feedback taps are chosen, however, the output sequence will have a periodicity of 2^{n-1}, because an n-bit register cannot cycle through the zero state (where the state is defined by its binary contents). Obviously as the table in (a) indicates, it is impossible for all the stages simultaneously to contain a 0, because once in this state no new state can be generated with the simple logic used.

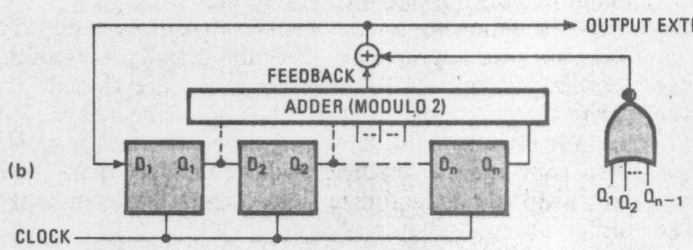
Most of the practical sequence generators therefore employ automatic detection of the 0 state on power up, in order to generate a logic 1 state at the output of one register, using a NOR gate as shown. After initialization, though, the random generator will cycle with a period of 2^{n-1}, because the 0 state never recurs. However, as shown in (b), the number of states cycled through can be increased to 2^n if the last input to the NOR gate is connected to the Q_{n-1} stage, instead of the output of the Q_n stage, and if the output of the NOR is connected to a summing port, instead of the set input being connected at the last flip-flop. The resulting m-sequence will now contain an equal number of 1s and 0s.

The logic needed to implement the summing port is small. In most cases, it need consist of a half-adder or a few resistors only. Note from the table in (b) that the all-zero state is detected and used to generate a logic 1.

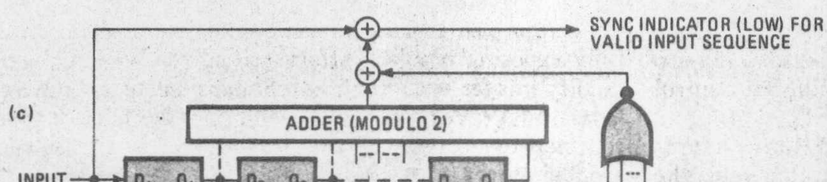
The same basic circuit can be used in the feed-forward mode to detect a sequence of n bits, too, as (c) proves. This method for checking the presence of a given sequence is of value when the error probability is low. During high-error bursts, however, the circuit's effi-



STATE	CONTENTS	FEEDBACK
1	00....1	1
2^{n-1}	10....0	depends on feedback circuit



STATE	CONTENTS	FEEDBACK	NOR	MODIFIED FEEDBACK
1	00.....1	1	1	0
0	00.....0	0	1	1
2^{n-1}	10.....0	depends on feedback circuit	0	depends on feedback circuit



Balanced states. The usual n-stage, pseudo-random number generator cannot generate an equal number of 1s and 0s because it cannot cycle through the register's all-zero state (a). Modified circuit cycles through all 2^n states (instead of the usual 2^{n-1} states) and detects 0s (b). Circuit can be used in feed-forward mode to detect repeating sequences (c).

3 ns per °C. This ensures equal temperature-dependent voltage drops across both optocouplers, and with them connected as shown, the temperature-generated voltages will cancel. The op amp's temperature coefficient is negligible in comparison and need not be considered. □

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Timer IC circuit separates rep rate and duty cycle control

by Arturo Sancholuz
Laboratorio Nacional de Hidraulica, Caracas, Venezuela

Combining both halves of a 556 dual timer with an operational amplifier in this simple circuit enables independent control of the output frequency and the duty cycle. The frequency is adjustable throughout the normal 10-hertz-to-10-kilohertz range of the 556, and the duty cycle is selectable from 1% to 99% of the total waveform period.

As shown in the figure, one half of the 556 (A_1) is connected as an astable multivibrator, oscillating at a frequency given by $f = 1.4/(R_1 + R_2)C$. This oscillator is the frequency-governing element in the circuit.

The negative-going edge of signal v_1 periodically triggers timer A_2, which operates as a monostable multivibrator. An exponential ramp emanating from the threshold port of A_1 drives A_2 through the 531 op amp.

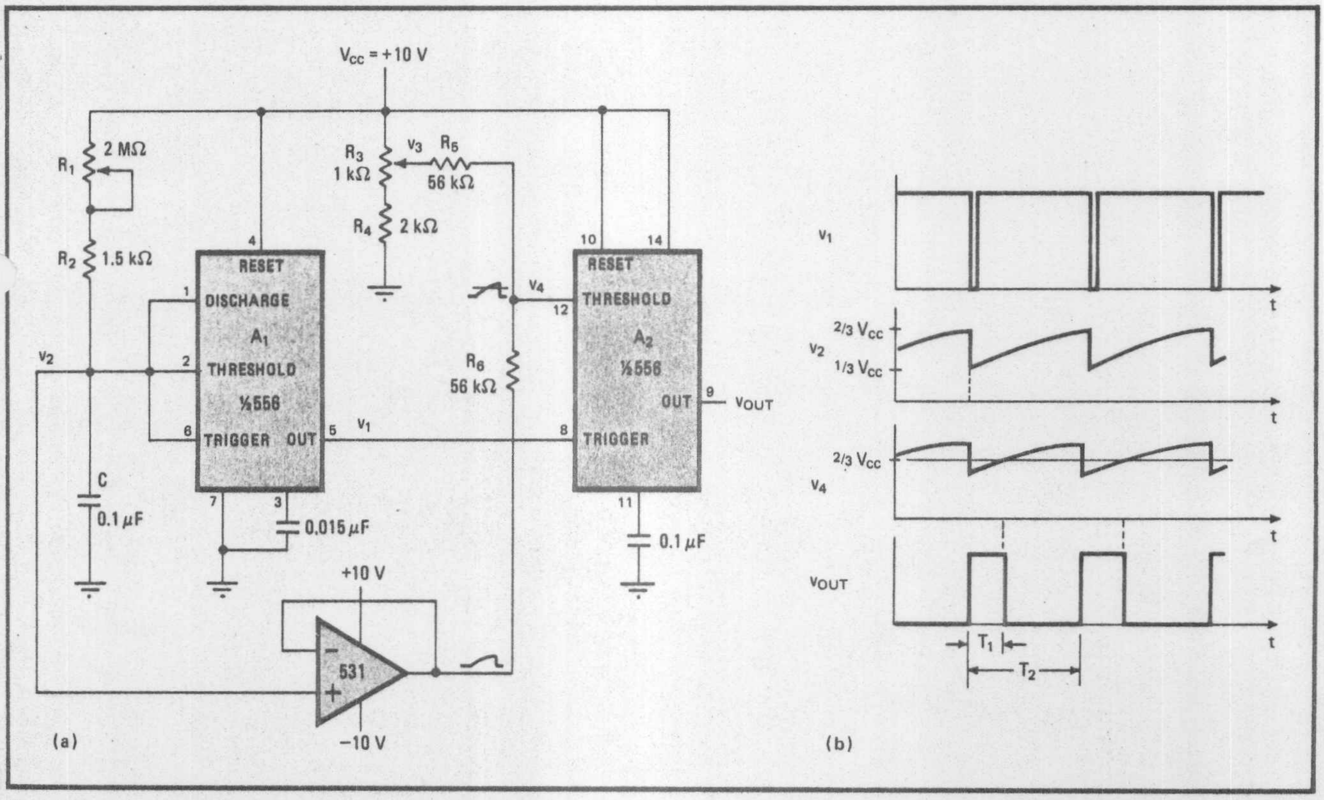
The duty cycle in this timer is determined not by external resistance-capacitance elements, but by the voltage on the threshold port. The output of A_2 will remain high if the threshold voltage stays below two thirds of the supply voltage, V_{cc}. This circuit can generate a dc offset voltage at the port to modify the threshold-switching time.

The voltage at the threshold port is determined by the two input voltages, v_2 and v_3, at the summing junction. Thus:

$$v_4 = v_2\left(\frac{R_5}{R_5+R_6}\right) + v_3\left(\frac{R_6}{R_5+R_6}\right)$$

Voltage v_2 is an exponential ramp resulting from charging C through resistances R_1 and R_2. The boundaries of the signal, determined by the internal comparators of A_1, lie between $\frac{1}{3}V_{cc}$ and $\frac{2}{3}V_{cc}$.

The 531 op amp is a buffer for the high-impedance A_2 signal and prevents current from flowing into the timing port, which could charge C from V_{cc} through R_5 and R_6. Dc voltage v_3 can be varied from $\frac{2}{3}V_{cc}$ to V_{cc}. Thus it can be seen that R_3 will determine how large a dc voltage is superimposed on v_2, thereby controlling the duty cycle. Since there are no feedback loops linking A_1 and A_2, it is clear that frequency and duty cycle adjustments are independent. □



No relation. A_1 runs at frequency set by R_1. But duty cycle is selected by R_3, which controls signal offset at threshold port of A_2. No feedback loops link A_1 and A_2, thereby ensuring independent adjustment of rep rate and duty cycle. Timing diagram details operation.